		,							
Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)					ATTY. DOCKET NO. 35955			SERIAL NO. 10/627,479	
					APPLICANT: Kazushi Higashi et al.				
በ ፡ ፲፻፫5 ፡፡					FILING DATE: July 25, 2003			GROUP ART UNIT: 4227 3729	
Title 1	-	4	U.S. PA	TENT DO	CUMENTS				
Examiner Initial		Document No.	Date	Na	ame	Class	Sı	ubclass	Filing Date
	Α								
	В								
	С								
	D								
	E				<u> </u>	,			
	F								
	G								
	Н								
			FOREIGN	PATENT I	OCUMENT	rs			
		Document No.	Date	Co	untry	Class	Sı	ubclass	Translation
	1						1	-	

Document No. Date Country Class Subclass Translation I 3-241755 10/1991 JP Eng. abstract & Partial Trans. Attached

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.) K "Development of chip-on-chip bonding process at a room temperature (with copper, a bumpless bonding is also possible)", Semiconductor Sangyo Newspaper, June 12, 2002, pg. 9, Sangyo Times Inc., Tokyo, Japan. L "Development of chip-on-chip bonding process at a room temperature by a superbonder", Electronic Materials, July 1, 2002, pp. 8-9, Vol. 41 No. 7, Kogyo Chosakai Publishing Co., Ltd., Tokyo, Japan. M "Ultrasonic Flip Chip Bonding Technology for LSI Chip with High Pin Counts" by Kajiwara et al., from Proceedings of the 7th Symposium on Microjoining and Assembly Technology in Electronics, February 1, 2001, pp. 16166, Japan Welding Society, Tokyo, Japan.

Examinera

. arbe

Date Considered

*Examiner:

Initial if reference considered, regardless of whether citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.